

# Claims

- [c1] A method for removing exposed seed layer in the fabrication of solder interconnects on electronic components such as semiconductors comprising the steps of:  
providing an electronic component having a plurality of spaced apart solder interconnects formed on a seed layer, the seed layer extending in the spaces between the solder interconnects and being exposed and the seed layer comprising a plurality of layers including a lower layer;  
removing the exposed layers above the lower layer using an etchant;  
rinsing the electronic component;  
contacting the rinsed component with an oxalic acid solution while the electronic component is still wet; and  
removing the exposed lower layer using an etchant.
- [c2] The method of claim 1 wherein the solder interconnects are made from a solder containing tin.
- [c3] The method of claim 2 wherein the seed layer comprises a lower TiW layer, an intermediate Cu/Cr layer and an upper Cu layer.

- [c4] The method of claim 3 wherein the intermediate Cu/Cr layer and upper Cu layer are removed using an electroetch process.
- [c5] The method of claim 4 wherein after contacting with the oxalic acid solution and rinsing, the rinsed electronic component is contacted with a methane sulfonic acid solution and rinsed before removing the lower TiW layer.
- [c6] The method of claim 4 wherein after rinsing the electronic component after the first etch, the rinsed component is contacted with a methane sulfonic acid solution before contacting with an oxalic acid solution.
- [c7] The method of claim 4 wherein the electroetch process is a horizontal process.
- [c8] The method of claim 4 wherein the electroetch process is a vertical process.
- [c9] The method of claim 1 wherein the solder interconnects are made from a lead free or substantially lead free solder containing Sn.